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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,093	12/18/2001	Frank Matthews	5646-36	4976

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EXAMINER	
DILLER, JESSE DAVID	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,093	MATTHEWS ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) 31-34 is/are allowed.

6)☒ Claim(s) *1-3,7,10-12,21,22 and 35* is/are rejected.

7)☒ Claim(s) *4-6, 8-9, 13-20, 23-30, 36-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/18/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 are pending in the case and have been examined.

Information Disclosure Statement

2. The Information Disclosure Statement filed on 12/18/2001 has been examined.

Specification

3. The abstract of the disclosure is objected to as being of excessive length.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The disclosure is objected to because of the following informalities:

- On Page 10, lines 5-9 and 26-30 conflict with Fig. 3. Page 10 teaches that the leading edges of the WR and MATCH signals are generated in sync with the transition of the R/W_1 and read address A1. However, Fig. 3 shows a very large time delay between these transitions and the leading edges of the signals.
- On Page 13, line 1, "36a, 36b" should be replaced by "34a, 34b."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites the limitation "the first output latch" in line 12. There is insufficient antecedent basis for this limitation in the claim. No "first output latch" was previously disclosed. For the purposes of prior art examination, the claim has been taken to read, "said bypass latch."

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 7, 10-12, 21-22, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito, US Patent #5,321,652.

10. As for claims 1, 10, and 21, Ito teaches:

- In an integrated circuit memory device (IC CHIP, Fig. 1) comprising a memory array (MARY, Fig. 6; Col. 3, lines 56-59) having first and second ports (MULTIPORT MEMORY, Fig. 1; Fig. 6) that can each support asynchronous read and write access (Col. 1, lines 26-41; Col. 13, lines 5-8) and a pulsed sense

amplifier (split multistage amplifier: RAB and DSL, Fig. 2) that receives data (dr0-drn, Fig. 2) from the second port (DB0-DBn, Fig. 6) a method of operating the memory device, comprising the steps of:

- writing first data (da0-dan, Fig. 6) from a data input buffer coupled to the first port (DBA, Fig. 6) to a write address in the memory array while simultaneously writing a copy of the first data to a bypass latch (CN1-6, Fig. 2) associated with the second port (Fig. 2 shows a copy of the first data da0-dan written to the input of the latched DSL);
- reading second data from a read address in the memory array by activating the pulsed sense amplifier (DSL, Fig 2) to latch the second data (Col. 8, lines 33-38); and
- overwriting the latched second data with the copy of the first data from *said bypass latch* (see 35 USC 112 2nd rejection of claim 1 above; before the assertion of match signal am, Fig. 2, the DSL outputs db0-dbn hold the latched second data dr0-drn. Upon the assertion of the match signal am, the latched second data dr0-drn at the output db0-dbn is overwritten by the first data da0-dan)

11. As for claim 2, Ito additionally teaches:

- the second data is latched in response to a leading edge of a latch enable signal (see DSL, Fig. 2; the latch is enabled by the match signal *am*; the second data is latched on the falling edge of *am*); and wherein

- the latched second data is overwritten with the copy of the first data from the bypass latch in response to a trailing edge of the latch enable signal (the rising edge of signal *am* latches the first data to overwrite the second data).

12. As for claim 3, Ito additionally teaches:

- the method of Claim 1, wherein said writing step comprises
- overwriting old data at the write address with new data; and wherein
- the second data latched by the pulsed sense amplifier is the old data (Fig. 5 teaches that *when there is coincidence of the read/write addresses,* dr0-drn holds old data at first; later, dr0-drn hold the new data read from the memory array. However, db0-dbn transitions to its final value before the transition of the read linesdr0-drn. As shown in Figure 2, on the falling edge of signal *am* until the rising edge, the data latched into the DSL is the data from the second port (DBA, Fig. 2). Therefore, before the final transition of the output lines db0-dbn to hold the first data, the sense amplifier had latched old data. Also see Col. 12, lines 24-30).

13. As for claim 7, Ito additionally teaches:

- comparing (AC, Fig. 2) the write address (aa0-aan) to the read address (ab0-abn); and generating a leading edge of a match signal if said comparing step indicates an equivalency (Col. 7, line 65 - Col. 8, line 6).

14. As for claim 11, Ito additionally teaches:

- said writing and reading steps occur asynchronously relative to each other (Col. 9, lines 12-15).

15. As for claim 12 and 22, Ito additionally teaches:

- generating a match signal in response to detection of an equivalency between the write address and the read address (Col. 7, line 65 - Col. 8, line 6).

16. As for claim 35, Ito teaches:

- A method of operating an asynchronous (Col. 9, lines 12-15) integrated circuit memory device (IC CHIP, Fig. 1) having first and second ports (MULTIPORT MEMORY, Fig. 1; Fig. 6) that can each support read and write access (Col. 1, lines 26-41; Col. 13, lines 5-8) to a memory array therein (MARY, Fig. 6; Col. 3, lines 56-59), said method comprising the steps of:
- writing new data from the first port to a write address in the memory array (Col. 10, line 57 – Col. 10, line 14) and a bypass latch associated with the second port (Fig. 6 shows the delivery of data to both the memory array and the bypass circuitry DSL);
- reading old data from a read address in the memory array to a sense amplifier associated with the second port (Col. 11, lines 15-34); and
- transferring the new data from the bypass latch to an output of the memory device (Col. 11, lines 39-61).2

Allowable Subject Matter

17. Claims 31-34 are allowed.

18. The prior art (Ito, US Patent #5,321,652) discloses a IC memory device using a multiported asynchronous memory, a sense amplifier, and a bypass circuit to allow simultaneous reads and writes to the same address. The prior art teaches that the output of the sense amplifier is connected to the input of the bypass circuit.

19. However, the prior art does not teach that the output of the bypass latch is connected to the sense amp's input. The prior art of record neither anticipates nor renders obvious the above-recited combination. Accordingly, the invention as claimed in claim 31 is not seen to be anticipated or made obvious, within the meaning of 35 USC 103, by the prior art of record. Therefore, claim 1 is deemed allowable.

20. Dependent claims 32-34 inherit the limitations of claim 31 and are allowable for the same reasons.

21. Claims 4-6, 8-9, 13-20, 23-30, and 36-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. The primary reason for allowance of claim 4 in the instant application is the combination with the inclusion in these claims that the bypass circuitry overwrites new data with new data. The prior art of record neither anticipates nor renders obvious the above recited combination.

23. The primary reason for allowance of claims 8-9, 13-20, 23-30, 36-38 in the instant application is the combination with the inclusion in these claims of a distinction between the match signal and latch enable/loopback signals. The prior art of record neither anticipates nor renders obvious the above recited combination.

24. If the applicant should choose to rewrite the independent claims to include the limitations recited in either one of claims 4-6, 8-9, 13-20, 23-30, 31-34, and 36-38, the applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

25. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the M.P.E.P.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ito, US Patent #5,197,035, discloses much the same subject matter as the prior art relied upon in the section entitled *Claim Rejections – 35 USC 102,* and has a priority filing date of Oct. 19, 1988. Okita, US Patent #6,181,634, also discloses a multiport memory device that uses match detection and bypass circuitry to

allow data flow-through. However, Okita discloses a synchronous dual-port memory with one read and one write port. Lindner, US Patent #5,761,147, discloses a virtual dual-ported memory which uses timing and circuitry to allow a single-ported memory to function as a dual-ported memory, which circuitry includes bypass circuitry to allow fast write-through. Proebsting, US Patent #5,999,478, discloses a tri-ported memory system with read bypass capability. Hsu, US Patent #6,445,638, discloses a dual-ported SRAM with flow-through capability.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571)272-4173. The examiner can normally be reached on 8:00AM-4:30PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JD

NASSER MOAZZAMI
PRIMARY EXAMINER

11, 23, 04